AMENDMENTS TO THE WRITTEN DESCRIPTION:

Please replace the paragraph beginning at page 10, line 5 with the following:

Similarly, Terminal #2 14 generates a Tx Clock 14d and Tx Data 14e using the Spread Spectrum Modulator 14b in a similar fashion described earlier for Terminal #1. Likewise, Terminal #1 ~~10~~ 12 may receive the RL signal via antenna 12a, and demodulate and track the signal as described earlier with receiver 12c to provide Rx Data 12f and Rx Clock 12g to the intended user.

Please replace the paragraph beginning at page 10, line 13 with the following:

Referring now to Figure 2 there is shown a simplified block diagram showing a representative DSSS transmitter system 2A - incorporating feature of the present invention. The transmitter includes a PN master clock 21, a PN code generator 22, a data clock generator 23, a data multiplexer 24, a modulo-2 combiner 25, a modulator 26, transmitter 27, and an antenna 28. The PN master clock 21 is used to generate the clock signals for the PN generator 22 and the data clock generator 23. The data clock generator 23 uses the master clock 21, the divisor N_c, and the XY-epochs to generate the desired data clock signal. The data clock signal is then used to drive the data multiplexer 24 to produce aggregate data d(t). The PN code generator 22 provides an aggregate PN code p(t) which is modulo-2 combined with the aggregate data d(t) from the multiplexer 24 to produce baseband signal s(t). The signal s(t) modulates the carrier using a mixer 26 and local oscillator, LO. The resultant modulated signal is transmitted via antenna 28 to the DSSS receiver 2B.

Please replace the paragraph beginning at page 11, line 30 with the following:

Referring also to Figure 3<u>A</u> there is shown a block diagram of the data clock generator 3B7 incorporating features of the present invention. The X-code generator 3B2 generates a binary 2^n PN code, where n=0,1,2,3...max. The Y- code generator 3B3 generates a maximal length code 2^m-1, where m is an integer value ≤ n. The Z-code generator 3B4 generates any suitable PN code to be combined with the X- and Y-codes in code combiner 3B5. Code combiner 3B5 may be any suitable code combiner such as a MAND code combiner or a MAJ code combiner, both of which are known in the art. The divide by N_c binary divider 3B8 divides the PN master clock 3B1 signal by a divisor N_c. Where N_c is determined by the prime factors of the binary and maximal-length PN code generators X and Y (and optionally Z) as shown in Figure 3<u>A</u>. In a preferred embodiment, the X binary code provides prime factor 2, and the Y code is selected to be of length 2^{12}-1 = 4095. The Y code of length 4095 contains prime factors: 3,3,5,7,13. Note that the prime factors are multiplied together to produce the code length, i.e. 4095 = 3x3x5x7x13. The set of possible divisor N_c values available using these code lengths can be obtained by generating the table shown in Figure 6. Figure 6 gives in tabular format the possible values of N_c for each combination of prime numbers: 2, 3, 3x3, 5,7,and 13. Stated differently, any value of N_c listed in Figure 6 may be used as PN master clock divisors. Each value of Nc in Figure 6 has the properties of generating synchronous symbol clocks that are edge coincident with the X- and Y- PN code epochs.

Please replace the paragraph beginning at page 13, line 23 with the following:

Still referring to ~~figure 3~~Figure 3A, the divide by N_c binary divider 3B8 is reset by XY epochs detected by AND gate 3B6 to transition from one data clock rate to a second data clock rate (for example: Figure 3C, t_1 to t_2). In the preferred embodiment the transition from one data clock rate to the second data clock rate is accomplished nearly simultaneously on the transmitter and receiver. In alternate embodiments any suitable logic circuit may be used to detect XY epochs and to reset the binary divider 3B8. Figure 3B shows the functional blocks of Figure 3A on an integrated circuit 32.

Please replace the paragraph beginning at page 14, line 6 with the following:

The X-code length is selected, step ~~42~~ 44 to be of length 2^n, for n=0,1,2,3...max. This code contains the prime number 2 and can be used to generate binary (2,4,8,...) data clock divisions that are leading edge coincident with the X-epoch. In alternate embodiments trailing edge coincidence may be used. The X-code is preferably generated by inserting a "1" (or "0") after the Y-code maximal length code 2^m-1 (see below); in this manner the invention advantageously minimizes hardware and exploits the auto- and cross-correlation properties of the PN codes. In alternate embodiments other codes having suitable auto-and cross-correlation codes could also be used.

Please replace the paragraph beginning at page 14, line 23 with the following:

Still referring to Figure 4, the prime factors of the maximal length code are determined, step 43. ~~The next~~ A subsequent step, 45, determines a divisor N_c by selecting a factor from the prime factorization of the maximal length Y-code $2^{max}-1$, and multiplying the factor by the binary X-code 2^n, n=0,1,2,3...max (see table 1 and example below). This PN code derived divisor N_c is then used to divide, step 46, the dividend, and the PN master clock (item 21 in Figure 2), to generate the data clock. It will be appreciated that deriving the data clock from the PN master clock in this manner ensures coincidence between a PN master clock cycle leading edge and a XY-epoch data clock cycle.